In the Claims

The following is a clean version of the entire set of pending claims :

1. **(Amended)** A method for transferring vector data in a computer system, the method comprising:

identifying use of vector data in an application program;

implementing at least one vector data instruction for transferring the vector data between a memory and a vector buffer, the vector data in the buffer being accessible by a processor in the computer system.

2. The method of claim 1 further comprising:

implementing a synchronization instruction to synchronize accessing the vector data with processing the vector data.

3. The method of claim 1 wherein the at least one vector instruction transfers data from the memory to the buffer.

4. The method of claim 1 wherein the at least one vector instruction transfers data from the buffer to the memory.

5. The method of claim 1 wherein the at least one vector instruction transfers data from the buffer to a general purpose register in the processor.

6. The method of claim 1 wherein the at least one vector instruction transfers data from a general purpose register in the processor to the buffer.

7. The method of claim 1 wherein the at least one vector instruction is used to determine whether the buffer is available for use.

8. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the starting address of the vector stream.

9. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the length of the vector stream.

10. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the stride of the vector stream.

11. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the starting address of the buffer.

12. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the width of the vector data in the data stream.

13. The method of claim 1 wherein the at least one vector instruction includes information about whether the vector data is integer or floating point data.

14. **(Amended)** A data processing system comprising:

a data processor, said data processor comprising:

a cache,

a register file, and

a vector buffer;

means for identifying use of vector data in an application program;

at least one vector data instruction for transferring the vector data directly between a memory and the buffer, the vector data in the buffer being accessible by the data processor; and

a synchronization instruction to synchronize accessing the vector data with processing the vector data.

15. The data processing system of claim 14 wherein the at least one vector instruction transfers data from the memory to the buffer.

16. The data processing system of claim 14 wherein the at least one vector instruction transfers data from the buffer to the memory.

17. The data processing system of claim 14 wherein the at least one vector instruction transfers data from the buffer to a general purpose register in the processor.

18. The data processing system of claim 14 wherein the at least one vector instruction transfers data from a general purpose register in the processor to the buffer.

19. The data processing system of claim 14 wherein the at least one vector instruction is used to determine whether the buffer is available for use.

20. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the starting address of the vector stream in the memory.

21. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the length of the vector stream.

22. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the stride of the vector stream.

23. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the starting address in the vector buffer.

24. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the width of the vector data in the data stream.

25. The data processing system of claim 14 wherein the at least one vector instruction includes information about whether the vector data is integer or floating point data.

26. The data processing system of claim 14 further comprising:

a vector transfer unit operable to perform burst transfers of the vector data based on the at least one vector instruction.

27. The data processing system of claim 14 wherein the means for identifying use of vector data in an application program is a compiler.

28. The data processing system of claim 27 wherein the compiler identifies use of the vector data based on whether the vector data is used in a program loop.

29. The data processing system of claim 14 wherein the means for identifying use of vector data in an application program includes a vector data indicator, the vector data indicator being recognizable by a compiler as indicating use of the vector data.

30. The data processing system of claim 29 wherein the compiler implements the at least one vector transfer instruction when the compiler recognizes the vector data indicator.

31. Cancelled.

32. Cancelled.

33. Cancelled.

34. Cancelled.

35. Cancelled.

36. Cancelled.

37. Cancelled.

38. Cancelled.

39. Cancelled.

40. Cancelled.

41. (New) A method comprising:

a compiler scheduling a transfer of a first stream of vector data between a processor and a memory; and

the compiler scheduling a transfer of a second stream of vector data between the processor and the memory so that the second stream of vector data is transferred while data of the first stream is processed.

42. (New) A computer-readable medium having stored thereon instructions which, when executed by a processor, configure the processor to:

schedule a first transfer of a first stream of vector data between the processor and a memory; and

schedule a second transfer of a second stream of vector data between the processor and the memory such that the second transfer occurs while data of the first stream of vector data is processed by the processor.

43. (New) The computer-readable medium of claim 42 which further configures the processor to:

schedule the first transfer of the first stream of vector data between a vector buffer of the processor and the memory; and

schedule the second transfer of the second stream of vector data between the vector buffer and the memory such that the second transfer occurs while data of the first stream of vector data is processed by the processor.

44. (New) The computer-readable medium of claim 43 wherein at least one of the first transfer and the second transfer is a burst transfer.

45. (New) The computer-readable medium of claim 43 which further configures the processor to:

partition vector data of a computer program into a plurality streams.

46. (New) The computer-readable medium of claim 42 which further configures the processor to:

detect vector data in a computer program.

47. (New) The computer-readable medium of claim 46 which further configures the processor to:

detect a vector data indicator in the computer program, the vector data indicator identifying the vector data.

48. (New) The computer-readable medium of claim 46 which further configures the processor to:

generate a vector instruction, wherein a stream of the plurality of streams is transferred from the memory to the vector buffer in response to execution of the vector instruction.

49. (New) The computer-readable medium of claim 46 which further configures the processor to:

generate a vector instruction, wherein a stream of the plurality of streams is transferred from the vector buffer to the memory in response to the execution of the vector instruction.

50. (New) The computer-readable medium of claim 46 which further configures the processor to:

generate a vector instruction, wherein a stream of the plurality of streams is transferred fom the vector buffer to a register of the processor in response to the execution of the vector instruction.

51. (New) The computer-readable medium of claim 46 which further configures the processor to:

generate a vector instruction, wherein a stream of the plurality of streams is transferred from a register of the processor to the vector buffer in response to the execution of the vector instruction..

52. (New) The computer-readable medium of claim 42 which further configures the processor to:

generate a synchronization instruction to synchronize the first and second transfers while the data of the stream of vector data is processed by the processor.